# Effects of Etching Current Density on Surface Characteristics of Palladium-Hosted Porous Silicon Structures

**Zhang Boo Wei, Ming Liao Dong, Yang Hu Liang**

College of Applied Sciences, National Taiwan University of Science and Technology, Taipei City, TAIWAN (R.O.C.)

**Abstract**
In this work, porous silicon layer formed by photoelectrochemical etching on the surface of p-type silicon substrate was decorated with palladium nanoparticles applied over the porous layer by the electrostatic injection technique. The porosity, porous layer thickness and pore diameter were found reasonably depending on the current density passing through the circuit used for the Photoelectrochemical etching process. However, both the porosity and porous layer thickness showed saturation limit at high current densities, while the pore diameter was found to increase continuously with increasing current density.

**Keywords:** Porous silicon, Etching technique, Nanoparticles; Palladium dopants
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## 1. Introduction

Palladium exhibits remarkable catalytic properties, particularly in facilitating hydrogenation and oxidation reactions. It readily absorbs hydrogen, forming palladium hydride, a unique property used in hydrogen storage and sensing applications [1]. Chemically, palladium is relatively inert but can form compounds with halogens, sulfur, and carbon [2]. Its electrical conductivity and ability to form alloys make it invaluable in electronics, jewelry, and catalytic converters for reducing harmful emissions in automobiles [3].

Palladium nanoparticles exhibit unique properties such as high surface area, excellent catalytic activity, and remarkable chemical stability, making them highly valuable in various applications [4-6]. They are widely used in catalysis for hydrogenation, oxidation, and carbon-carbon coupling reactions, as well as in sensors, fuel cells, and biomedical fields. Their small size and quantum effects enhance their performance in energy conversion and storage [7,8].

The electrostatic injection technique is a versatile method for embedding nanoparticles into porous structures with high precision and uniform distribution [9-11]. This technique utilizes electrostatic forces to drive charged nanoparticles into the pores of a substrate [12,13]. A nanoparticle suspension is typically exposed to an electric field, which directs the charged particles toward the porous material, ensuring efficient penetration and adhesion within the structure. This method offers advantages such as controlled loading, minimal agglomeration, and enhanced nanoparticle integration [14,15]. It is widely used in applications like catalysis, drug delivery, and sensor fabrication, where the uniform embedding of nanoparticles significantly improves performance and functionality [16-18].

## 2. Experimental Work

Figure (1) shows schematically the experimental stages of preparation of porous silicon layer on the p-type silicon substrates, the electrostatic injection of palladium nanoparticles on the prepared porous silicon layer, and finally the architecture of the fabricated PANI-coated Pd-decorated porous silicon structure.

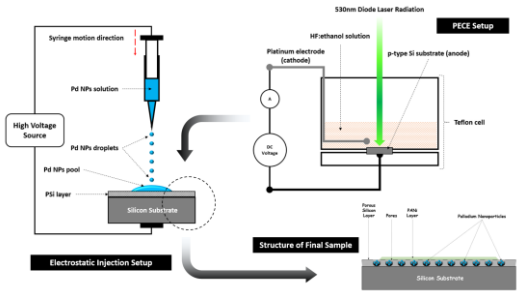


**Fig. (1) Schematic diagram of the experimental setup stages used in this work to prepare PANI-coated Pd-decorated porous silicon structure formed on p-type Si substrate**

To prepare palladium nanoparticles using the chemical reduction method, the following experimental procedure is typically employed. Palladium precursor (e.g., palladium chloride, $PdCl_2$), reducing agent (e.g., sodium borohydride, ascorbic acid, or hydrazine), stabilizing agent (e.g., polyvinylpyrrolidone (PVP) or citrate), and a solvent (usually water or ethanol) were used. A $10^3$ M concentration of the palladium salt is dissolved in the chosen solvent to form the precursor solution. The solution is stirred to ensure complete dissolution. A stabilizing agent is added to the precursor solution to prevent the aggregation of nanoparticles and maintain

  

stability during synthesis. The reducing agent is prepared separately and added dropwise to the precursor solution under constant stirring. The reduction reaction converts $Pd^{2+}$ ions into palladium atoms, which nucleate and grow into nanoparticles. The reaction is typically carried out at room temperature or slightly elevated temperatures, depending on the reducing agent used. The pH of the solution may be adjusted to optimize the reaction. The progress of nanoparticle formation can be monitored using techniques like UV-visible spectroscopy, where the characteristic surface plasmon resonance (SPR) peak indicates the presence of palladium nanoparticles. The nanoparticles are separated by centrifugation, washed with solvents (e.g., ethanol or water) to remove unreacted precursors and byproducts, and then dried under vacuum or at room temperature. This method is simple, cost-effective, and produces nanoparticles with controlled sizes and shapes suitable for various applications, such as catalysis and sensing.

The etched wafer was thoroughly rinsed with ethanol and deionized water to remove residual HF and other byproducts. The wafer was dried using nitrogen gas or air-drying. This method allows precise control over the pore size, depth, and porosity, making it suitable for applications in sensors, optoelectronics, and biomedical devices. A polyaniline (PANI) layer was applied over the Pd-decorated PSi layer to enhance its stability and protect it from environmental factors like humidity, oxidation, and contamination. The PANI layer acts as a protective coating, preserving the catalytic properties of palladium while preventing degradation and improving the longevity of the device.

### 3. Results and Discussion

The features of bare PSi layers such as the pore shape, their dimensions and wall sizes between neighboring pores depend intensively the applied current density. The increase in pore size has also led to an overlapping of the pores which disfigured their shapes. The accumulation of electron-hole pairs within the porous layer may be responsible for the pore diameters [19]. By increasing the etching current density, the pore diameters increased. It ranged between 0.4 and 3.4 μm as the current density was ranging from 10 to 40 mA/cm$^2$ with 30% distribution of 1.64 μm. The porosity (P%) of the porous silicon layer after etching was calculated gravimetrically using the following equation:

$$P(\%) = \frac{m_1 - m_2}{m_1 - m_3} \quad (1)$$

where $m_1$ is the weight of silicon substrate before etching, $m_2$ is the weight after etching, and $m_3$ is the weight after removing the porous silicon layer by treatment the sample with 5 M NaOH for 5 min

The thickness (d) of porous silicon layer can be determined by the following equation:

$$d = \frac{m_1 - m_3}{A \times W} \quad (2)$$

where A is the surface area of the etched silicon surface, and W is the density of silicon

The increase in current density led to variation in the surface density of the pores within the porous matrix. The density of pores represents the number of pores per unit area. This surface density can be considered as a nucleation and growth sites for reduction of $Pd^{2+}$ to Pd nanoparticles ($Ag^{2+} + 2e^- \rightarrow$ Pd) and hence the development of the porous structure. As the pores density increased, the density of Pd reduction sites (Si-$H_x$) bonds increased. This led to an increase in the density of the Pd nanoparticles, which acts as a plasmonic active element to improve the SERS intensity [20].

Porosity, layer thickness, and pore diameter are the most common parameters used to evaluate the quality of the porous structure. These properties depend on the etching conditions, including etching current density, etching time and luminosity characteristics of the laser used for irradiation. Figure (2) shows the variation of porosity of the porous silicon layer with current density passing through the etching circuit. The porosity has increased 30% when the current density is 10 mA/cm$^2$ to 80% at 30 mA/cm$^2$. Beyond 30 mA/cm$^2$, the further increase in current density did not lead to corresponding increase in the porosity due to the saturation effect in the formation process of pores over the surface of silicon substrate.

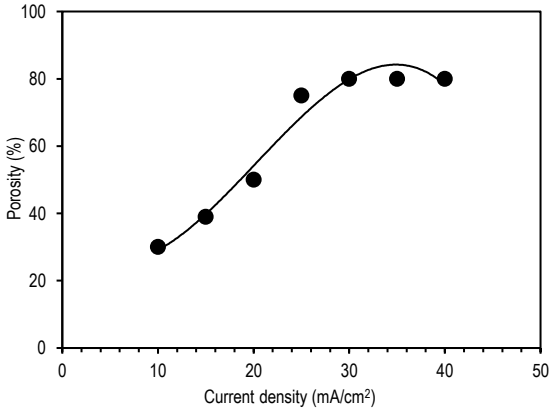


**Fig. (2) Variation of porosity of the porous silicon layer with current density passing through the etching circuit**

Similar behavior to that seen in Fig. (2) can be seen in Fig. (3), which shows the variation of thickness of the porous silicon layer with current density passing through the etching circuit. A relatively rapid increase in the porous layer thickness from 3 to 8.5 μm was observed when the current density was increased from 10 to 30 mA/cm$^2$. With increasing current density beyond 30 mA/cm$^2$, a slow increase in the layer thickness was observed to appear approximately constant (8.5-8.7 μm). This is also attributed to the saturation effect in the growth of the pores within the porous silicon layer.

  

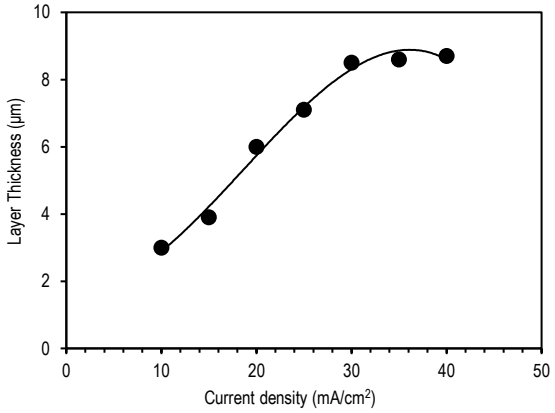


**Fig. (3) Variation of thickness of the porous silicon layer with current density passing through the etching circuit**

The pore diameter is very important parameter in the decoration of porous silicon structures with nanoparticles as the embedment of nanoparticles inside the pores principally depends on the diameters of both pore and nanoparticle. Figure (4) shows the variation of pore diameter within porous silicon layer with current density passing through the etching circuit. It was expected that the pore diameter would show the same behavior seen for the porosity and layer thickness. However, the pore diameter has continuously increased from 0.4 to 3.4 μm with current density increasing from 10 to 40 mA/cm$^2$. This continuous increase is ascribed to the decrease in the thickness of pore walls to grow radially towards the neighbor volume. When the pores are separated by small distances, they may collapse into each other with the continuous increase in pore diameter. This will lead to form larger pores, which have advantages and disadvantages depending on the architecture of the porous structure to be prepared.

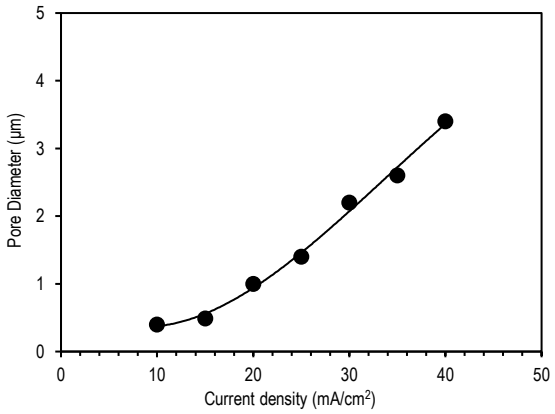


**Fig. (4) Variation of pore diameter within porous silicon layer with current density passing through the etching circuit**

## 4. Conclusion

In concluding remarks, porous silicon layer formed by photoelectrochemical etching on the surface of p-type silicon substrate was decorated with palladium nanoparticles applied over the porous layer by the electrostatic injection technique. The porosity, porous layer thickness and pore diameter were found reasonably depending on the current density passing through the circuit used for the photoelectrochemical etching process. However, both the porosity and porous layer thickness showed saturation limit at high current densities, while the pore diameter was found to increase continuously with increasing current density.

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