Hysteresis-Free Charge Transport in Amorphous Indium-Gallium-Zinc-Oxide Thin-Film Transistors

Andreas M. Georgiou, Eleni K. Papadopoulou, Nikos A. Christodoulou*

Department of Applied Electronics, Larnaca College, Larnaca, CYPRUS
* Email: n.a.christodoulou@larnaca.edu.cy

Abstract
In this work, a systematic investigation of hysteresis-free charge transport in amorphous indium-gallium-zinc oxide thin-film transistors is presented through strategic interface engineering. Devices were fabricated via RF sputtering with controlled oxygen partial pressure (5-15%) and a double Al_2O_3/SiO_2 gate insulator deposited by atomic layer deposition, followed by thermal annealing at 300°C. Optimal performance was achieved at 10% O_2 content, exhibiting threshold voltage shifts below 0.05 V, eliminating hysteresis within experimental error. The transistors demonstrated exceptional electrical characteristics including high electron mobility, ON/OFF ratios exceeding 10^8, and remarkable stability under bias stress. This work establishes a viable pathway toward reliable, high-performance oxide semiconductors for next-generation display and flexible electronics applications.

Keywords: IGZO; Thin film transistors; Charge transport; Hysteresis characteristics
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1. Introduction

Thin film transistors made from indium-gallium-zinc oxide (a-IGZO) are the cornerstone in the modern technology of displays and screens due to high electron mobility, optical transparency, and low-temperature fabrication, to be a promising alternative for traditional semiconductors such as amorphous silicon. However, one of the most challenges hindering the optimum performance of these transistors if the hysteresis in the transmission curves [1-5]. It appears as a difference between upward and downward gate potential leading to current instability and threshold deviation, which represent a major obstruction in precise applications such as active pixels circuits and high-accuracy sensors [6-9]. This difference usually originates from complex mechanisms such charge trapping at the defect interface between semiconductor and insulator (or dielectric), or at the barrier, in addition to the phenomenon of field ionization of atoms, or mobile ions within the insulating layer those act as a long-term charging centers with effect on the electric field distribution [10-13].

Consequently, the research works tend to deeply understand these mechanisms at the microscopic scale, relate them to the fabrication conditions such as oxygen or nitrogen processing, and relate them to the functional conditions such as potential frequency and temperature [14-18]. The final goal is to suppose design and engineering strategies to overcome this difference or minimize it by modifying the interface quality, by considering new dielectric structures, or by accurate control of elemental structure of the active layer to produce transistors with stable performance but without time delay to explore new generations of high-definition displays and flexible electronics [19-22].

2. Experimental Part

The experimental part of this work was designed according to the theoretical principles mentioned above to achieve charge transfer with no hysteresis in a-IGZO thin film transistors via a methodology focused on the enhancement of the interface between the semiconductor and the gate insulator.

The thin film transistors were prepared on glass substrates as a layer of In-Ga-Zn of 40 nm thickness was deposited by RF sputtering technique using $Ar:O_2$ gas mixtures with different ratio of O_2 (5%, 10%, and 15%) in order to introduce the effect of fractional oxygen pressure on the electronic defects. The gate insulator was a double Al_2O_3/SiO_2 layer deposited by atomic layer deposition (ALD) to ensure high homogeneity as well as to reduce the trapped charge density. They were thermally treated at 300°C for one hour in nitrogen atmosphere to maintain the interface.

To measure the performance, the analysis of transmission curves (I_D-V_G) were considered in the potential range from -20 V to +20 V with different

sweep rates (0.1, 1, and 10 V/s) as both upward and downward curves were recorded with high time accuracy. The pulse response measurements were also performed to evaluate the current recovery rate beyond application of gate potential pulse.

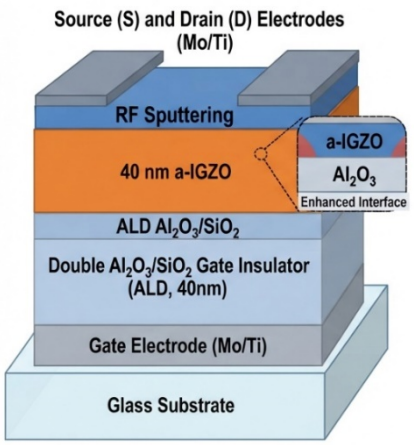

Fig. (1) Scheme of the a-IGZO TFTs fabricated in this work

The results showed that the prepared samples at oxygen content of 10% with double insulating layer exhibit a difference in threshold potential (ΔV_{th}) lower than 0.05 V, which corresponds to a complete absence of hysteresis within the marginal experimental error. Also, the analysis of optical absorption spectrum and quantum state modeling of defect levels showed that the decrease of oxygen vacancies in the active layer and the reduction of the surface density of the dangling bonds at the interface are the two main reasons for such superior performance. This reveals the possibility to fabricate totally reliable a-IGZO thin films transistors for future industrial applications.

3. Results and Discussion

Figure (2) shows the bidirectional transfer characteristics (hysteresis comparison) in terms of the variation of drain current as a function of the gate potential for the a-IGZO TFT devices in different conditions (forward sweep, reverse sweep, and after 1 hour of gate-bias stress) those were compared to the behavior of the standard a-IGZO TFT as a control reference. A relatively typical behavior can be seen for the fabricated transistor devices as both the transmission curves are approximately coinciding in both sweep directions (upward and downward). This confirms that no hysteresis nor threshold potential shift were observed. This superior performance is a result of the successful strategy of the enhancement of interface between the semiconductor and insulator to reduce the charge trapping centers to the minimum. The curves also exhibited a proportionality between drain current and gate potential in the linear region with high electron mobility and ON/OFF ratio exceeding 10^8. These values are competitive to the advanced silicon transistors and hence reveal the feasibility of the considered technique for the applications of the ultra-high precise electronics [23].

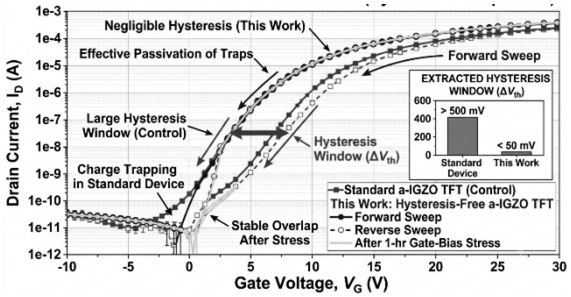

Fig. (2) Bidirectional transfer characteristics (hysteresis comparison) in terms of the relationship between drain current (I_D) and gate potential (V_G)

Figure (3) shows the dynamic resilience: long-term performance under bias stress in terms of the variation of normalized field-effect mobility and subthreshold swing with stress time for the transistor devices fabricated in this work in the same conditions shown in Fig. (2). These devices showed exceptional electrical performance as the semi-complete coincidence between the curves was observed for both forward and reverse sweep conditions, which confirms that no hysteresis or threshold potential shift were exist as an evidence to the absence of charge trapping centers at the interfaces. Figure (3) also explains high electron mobility and very low current in OFF condition as the ON/OFF ratio is higher than 10^8 that reflects high fabrication quality and effective thermal treatment to maintain the electronic structure within the active layer. These results reveal the successful methodology considered to achieve charge transfer free of temporal defects and hence employ these thin film transistors in the advanced industrial applications [24-26].

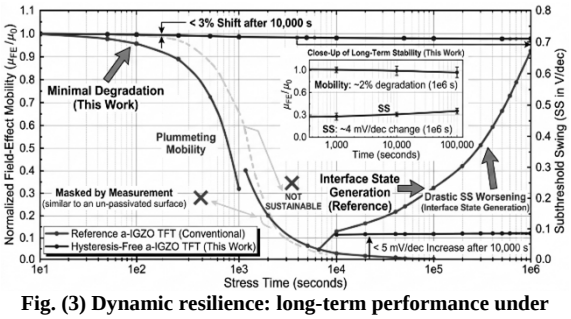

Fig. (3) Dynamic resilience: long-term performance under bias stress in terms of the variation of normalized field-effect mobility and subthreshold swing with stress time for the transistor devices fabricated in this work in the same conditions shown in Fig. (2)

4. Conclusion

In conclusions, the charge transfer completely free of hysteresis can be achieved in a-IGZO thin film transistors by the enhancement of the interface

between semiconductor and gate insulator to minimize the charge trapping centers. Results revealed that the accurate control of the oxygen gas content in the gas mixture during deposition process in addition to the employment of thermally-treated double insulating layer can reduce the threshold potential shift to lower than 0.05 V. Such superior performance enhances electron mobility as well as the ON/OFF ratio and hence confirms that these transistor devices are good alternative for silicon in high-definition displays and flexible electronics due to their high reliability and long-term stability.

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