Characteristics of CoO/Si Heterostructure Prepared by Plasma-Induced Bonding

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Abstract
In this work, the characteristics of the CoO-Si structure produced by plasma-induced bonding technique were studied. The produced structure was an asymmetric heterojunction consisting of n-type CoO on a p-type silicon substrate. The Si substrate and CoO sample were bonded by subjecting them to the plasma formed between two electrodes. The measurements included the structural and electrical characteristics. The built-in potential of the produced heterojunction is about 0.9eV with typical spectral responsivity within the range 300-900 nm. With dark current of 50μA, maximum reverse bias current of 180μA and ideality factor of 1.18, the results explained better characteristics than those of the same heterojunction produced by thermal evaporation technique.

Keywords: Cobalt oxide; Heterojunction; Plasma-induced bonding; Electronic transport; Semiconductors
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1. Introduction

There are many factors governing the bonding behavior of two surfaces. First, the surfaces must be flat and smooth. Usually it is argued that surfaces can make contact only at some asperities. However, the success of bonding technique has followed the development of modern semiconductor chemical-mechanical polishing (CMP) technology. The semiconductor polishing technology has reached such a level of maturity that, nowadays, commercial silicon wafers have surface roughness in the order of 10^{-10}m. The second parameter governing the ability for bonding is the surface chemical state and surface termination. For most semiconductors, surface preparation and cleaning techniques are well-developed and characterized. However, in silicon technology the surface chemical treatments are more standardized and established processes, as compared to, for example, compound semiconductors.

The basic procedure in semiconductor bonding technique starts with mirror-polished surfaces that are cleaned, plasma-activated and given their final surface termination using a combination of chemical treatments. The wafers are then brought together at room temperature and if proper surface conditions apply, the solids will bond spontaneous. After room temperature bonding, a heat treatment at elevated temperature is performed to strengthen the interface bonding. Typical bonding technique procedures are fully compatible with microelectronic process technologies, offering several advantages both in available processing equipment and possible applications.

When the solids have been bonded together at room temperature usually the interaction, or bonding energy, is relatively weak. Therefore, a heat treatment is performed to increase the bond-strength. The annealing enhances out-diffusion of interface trapped molecules and desorption of chemisorbed surface atoms, such as hydrogen. At the same time the annealing activates formation of covalent bonds between the bonded surfaces, like solid-to-solid bonding in the case of hydrophobic bonding. The thermal treatment used to increase the bond-strength can, unfortunately, also cause severe problems in bonding technique. For instance, when bonding dissimilar materials, the thermal mismatch induced high stresses in the

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material. High temperature annealing also restricts the use of metal patterns and can cause diffusion of dopants.

Generally, the bonding requires a high-temperature annealing step to ensure the formation of strong bonding between solids, i.e. to form covalent bonds. In silicon-to-silicon bonding usually an annealing above 1000°C is required, and in bonding involving compound semiconductors, the annealing is usually performed above 600°C. Such a high-temperature annealing is incompatible with many applications. Particularly, pre-structured wafers that already contain temperature-sensitive structures cannot be exposed to the high-temperature annealing. The high-temperature annealing also induces material degradation. It can cause broadening of diffusion layers. When bonding dissimilar materials, annealing at high temperatures would induce large thermal stress due to the difference in thermal expansion coefficients [5-10].

In this work, the use of plasma activation of the surfaces before bonding has been examined to achieve a low-temperature bonding.

2. Experimental Part

High purity (99.999) (100)-oriented p-type silicon wafers of 500μm thickness and 3 Ω.cm resistivity were used in this work. Also, high purity (99.999) cobalt oxide (CoO) was used to form 350μm-thick samples. Both samples, Si and CoO, were washed with distilled water then rinsed in ethanol and subjected to ultrasonic waves for 10 minutes, then dried by hot air. The silicon samples were then cleaned with HF for 5 minutes to remove any residual oxides which have existed on their surfaces. Both samples were softly grinded and polished to obtain flat surfaces. Then, these samples were rinsed in ethanol to remove acids then dried to be ready for processing. The Si and CoO samples were mounted inside the plasma system, which is working under vacuum at room temperature. Discharge voltage and current are 15 kV_{DC} and 3 A, respectively. Argon gas at a pressure of (1 mbar) was used to generate the discharge plasma.

Electrical measurements were carried out using a dc power supply and digital electrometer while the C-V measurements were performed using *hp*/4192 ALF LCZ device. The samples were subjected heating up to 600°C within 5 minutes then left to return to its initial temperature within the same period of time.

3. Results and Discussion

If two identical solids with the same orientation are bonded together without misalignment and without interface contamination, they should merge into one. However, there are always deviations from the ideal case. In the bonding technique, there is always an unavoidable misalignment between the bonded solids and therefore misfit dislocations appear. Misfit dislocations will also appear at the bonded interface if two solids of different orientation or different lattices are bonded. The presence of native oxides, adsorbed surface contaminants and interface bubbles (voids), also inhibit a perfect solid-to-solid transition region. Figure (1) explains the structure of the bonded samples where the misfit in the CoO-Si interface is shown.

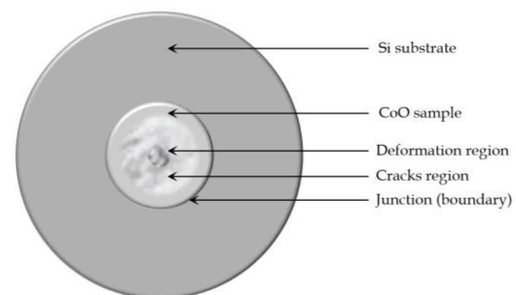

Fig. (1) The structure of the bonded CoO and Si samples

Defect-etching techniques were found to be more suited for investigations of bulk material defect introduced by the bonding technique, arising mainly from thermal mismatch stress. Defect-etching uses etch selectivity to reveal crystal imperfection such as dislocation. The dislocation appears

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as pits on CoO surface and their origin is traced from the shape of the pits, as shown in Fig. (1). For Si and other semiconductors, defect-etching techniques are well developed and frequently used.

Wafer bonded p-n heterojunction characteristics are heavily affected by the non-ideal interface. However, a substantial improvement of wafer bonded p-n heterojunctions characteristics is usually obtained by shifting the p-n transition away from the bonded interface, either by high temperature annealing [17-18] or by implantation [19-20]. Alternatively, the p-n heterojunction formed under UHV conditions and low temperatures results in an ideality factor no more than 1.18 and indicates low recombination at the interface. Bonding p-n heterojunction in ambient air and subsequent high temperature annealing was seen to yield high recombination near the bonded interface. An ideality factor of 2 was obtained and low minority carrier lifetime [21]. Figure (2) shows the I-V characteristics of bonded p-n Si-CoO heterojunction.

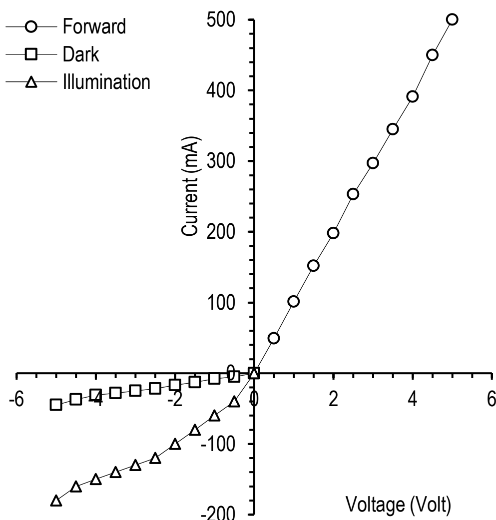

Fig. (2) The I-V characteristics in dark and light for the CoO-Si heterojunction

As shown, the dark current is about 50μA and the forward current is uniformly linear. The illumination current in the reverse biasing reaches a maximum of about 180μA. The bonded interface is often avoided in the electrically active region of the electronic device. However, the recombination centers of the defective bonded interface are used to control the minority carrier lifetime in power devices. These characteristics are typically enhanced compared to results obtained by another techniques [22] and Table (1) shows a comparison among the parameters of three different techniques (thermal evaporation, DC sputtering and plasma bonding).

Table (1) electrical parameters of the CoO/Si heterojunction prepared by different techniques

Technique	Dark Current (μA)	Maximum Reverse Current (μA)	Built-in Potential (eV)	Ideality Factor
Evaporation	80	140	1.2	0.6
DC sputtering	65	110	0.8	0.82
Plasma bonding	50	180	0.9	1.18

In order to introduce the nature of the anisotype CoO-Si heterojunction, the C-V measurements were performed in the reverse biasing and results are presented in Fig. (3). The built-in potential was determined for the CoO-Si heterojunction to be about 0.9 eV.

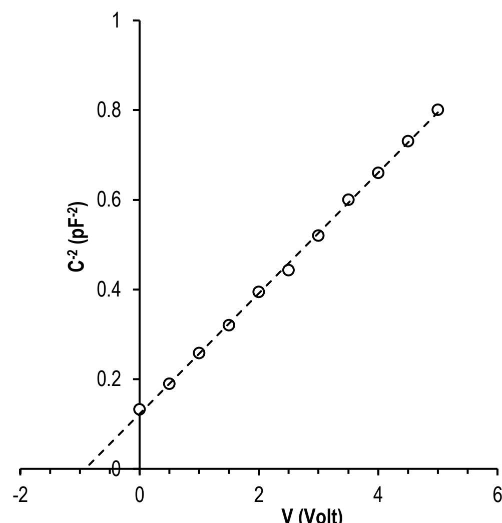

Fig. (3) The C-V characteristics of the CoO-Si heterojunction. The value of V_{bi} is about 0.9eV

4. Conclusions

A CoO-Si heterojunction was produced by plasma-induced bonding techniques. The structural characteristics explained the good bonding interface between the CoO and Si samples. Electrical measurements showed reasonable enhancement in the heterojunction characteristics compared to that produced by another techniques. Despite the complexity imposed by the

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plasma processing system, production of heterojunctions with such enhanced characteristics has advantages of low cost and large size devices.

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